

United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,825	07/01/2003	Fabrizio Simone Rovati	851763.434	3917
500	7590 11/28/2006		EXAMINER	
	ELLECTUAL PROPE	WOOD, WILLIAM H		
701 FIFTH A SUITE 5400			ART UNIT	PAPER NUMBER
SEATTLE,	SEATTLE, WA 98104			
			DATE MAILED: 11/28/2006	5

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
Office Anti-us Communication	10/612,825	ROVATI ET AL.				
Office Action Summary	Examiner	Art Unit				
	William H. Wood	2193				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on 01 Ju	ıly 2003.					
	action is non-final.					
3) Since this application is in condition for allowar	ince this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4) Claim(s) <u>1-18</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-18</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9)☐ The specification is objected to by the Examiner.						
10)⊠ The drawing(s) filed on <u>01 July 2003</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)						
1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)						
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Da	te				
3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 10/29/03;7/1/03. 5) Notice of Informal Patent Application 6) Other:						
	-/					

DETAILED ACTION

Claims 1-18 are pending and have been examined.

Information Disclosure Statement

1. The information disclosure statements (IDS) submitted on 01 July 2003 and 29 October 2003 were considered by the examiner.

Biglari-Abhari, M. et al., "Improving Binary Compatibility in VLIW Machines Through Compiler Assisted Dynamic Rescheduling" is not considered as a copy of the reference is not in the application.

Priority

2. Applicant has not complied with the requirements of 37 CFR 1.63(c), since the oath, declaration or application data sheet does not acknowledge the filing of any foreign application. A new oath, declaration or application data sheet is required in the body of which the present application should be identified by application number and filing date.

The identified priority document does not correspond to the provided certified priority document.

Oath/Declaration

Application/Control Number: 10/612,825 Page 3

Art Unit: 2193

3. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because: The clause regarding "willful false statements ..." required by 37 CFR 1.68 has been omitted.

Claim Rejections - 35 USC § 112

- 4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

 The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 5. Claims 1-11 and 16-18 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 recites numerous examples of "said order" (lines 10, 12 and 18), which are not clear. Under the "compiling" limitations and then the "ordering" limitation there are steps to "order" the bundles. Occurrences of "said order" need to clearly indicate which order. Dependent claims do not correct the issue. Claim 4 is unclear for phrase "detecting when one between". It is not clear to what "one" refers. Claim 16 refers to "said instruction stream" (line 3); there is insufficient antecedent basis for this limitation. The dependent claims do not correct the issue.

Application/Control Number: 10/612,825

Art Unit: 2193

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Menezes (USPN 6,950,926).

Claim 1

Menezes disclosed a process for executing programs on at least one processor having a given instruction set architecture, characterized in that it comprises the operations of:

compiling the program to be executed and translating said program into native instructions of said instruction set architecture, organizing the instructions deriving from the translation of said program into respective bundles arranged in order of successive bundles, each bundle grouping together instructions adapted to be executed in parallel by said at least one processor (column 3, lines 24-31; column 5, lines 2-4, "concurrently");

ordering said bundles of instructions in respective sub-bundles, said sub-bundles identifying a first set of instructions, which must be executed before the instructions belonging to the next bundle of said order, and a second set of instructions that can be executed both before and in parallel with respect to the instructions belonging to said next bundle of said order, it being possible for at least said second set of instructions to be the null set (column 4, lines 16-27; column 4, line 60 to column 5, line 6; column 5, line 59 to column 6, line 15; sub-bundle being instructions in first set required to execute before the second set/bundle);

defining a sequence of execution of the instructions of said sub-bundles in successive operating cycles of said at least one processor, while preventing, in assigning each sub-bundle to an operating cycle of the processor, simultaneous assignment, to the same operating cycle, of two sub-bundles corresponding to instructions belonging to said first set of two successive bundles of said order *(column 6, lines 11-15)*; and

Art Unit: 2193

executing said instructions on at least one said processor respecting said execution sequence (column 3, line 22).

Claim 2

Menezes disclosed the process according to claim 1, characterized in that it comprises the operation of selectively varying the overall length of instruction executed for each cycle by said at least one processor *(column 3, line 4, VLIW)*.

Claim 3

Menezes disclosed the process according to claim 1, characterized in that it comprises the operation of identifying the instructions belonging to a subbundle of said first set and of said second set by means of a binary symbol set at a first logic value and a second logic value, respectively (column 4, lines 28-43, the neutral instructions).

Claim 4

Menezes disclosed the process according to claim 3, characterized in that it comprises the operations of:

detecting when one between said first set and said second set is the null set (column 4, line 62 to column 5, line 1); and

inserting in the respective sub-bundle a fictitious instruction which does not imply any execution of operations (column 3, line 60 to column 4, line 15;

figure 1).

Claim 5

Menezes disclosed the process according to claim 1, characterized in that it comprises the operation of identifying the instructions belonging to a subbundle of said first set and of said second set by means of two distinct binary symbols which identify the last instruction of the respective sub-bundle (column 4, lines 13-15, "succeed ... the set"; column 4, lines 28-43, opcode and operand of the neutral instructions).

Claim 6

Menezes disclosed the process according to claim 1, for executing programs on a multiprocessor system comprising a plurality of processors having said instruction-set architecture (column 1, lines 14-17, multiple execution units), characterized in that it comprises the operations of:

instantiating the processors of said plurality with respective degrees of parallelism of execution with at least two different values of said parallelism of execution in the context of said plurality (column 1, lines 49-54; multiple execution units might all be executing in parallel or maybe just some are executing in parallel); and

selectively distributing execution of the instructions of said sequence of execution among the processors of said plurality, the instructions of said

Art Unit: 2193

sequence of execution being directly executable by the processors of said plurality in conditions of binary compatibility (column 1, lines 14-17, multiple execution units; column 1, lines 49-54; distributed to the multiple execution units).

<u>Claim 7</u>

Menezes disclosed the process according to claim 6, characterized in that it comprises the operation of selectively distributing the execution of the instructions of said sequence among the processors of said plurality, dynamically distributing the computational load of said processors (column 1, lines 14-17, multiple execution units to be selected for the instructions).

Claim 8

Menezes disclosed the process according to claim 6, characterized in that it comprises the operation of selectively distributing the execution of the instructions of said sequence among said processors of said plurality with the criterion of equalizing the operating frequency of the processors of said plurality (column 1, lines 14-17, multiple execution units).

Claim 9

Menezes disclosed the process according to claim 6, characterized in that it comprises the operation of performing a process of control executed by at least

Art Unit: 2193

one of the processors of said plurality so as to equalize its own workload with respect to the other processors of said multiprocessor system (column 1, lines 14-17, multiple execution units; figure 3, elements 201 and 203, equalized with respect to each other).

Claim 10

Menezes disclosed the process according to claim 9, characterized in that it comprises the operation of drawing up a table accessible by said control process, said table having items chosen from the group made up of:

a list of processes that are being executed or are suspended on any processor of said plurality of processors (column 6, lines 11-15);

the progressive number thereof according to the order of activation;

the percentage of maximum power of the processor that is used by said process;

the execution time;

the amount of memory of the system used by said process to be able to execute the function for which it is responsible;

the processor on which the process currently resides; and the address of the portion of memory in which the data and the instructions are stored (column 6, lines 29-45).

Claim 11

Application/Control Number: 10/612,825

Art Unit: 2193

Menezes disclosed a processor system, preferably of a multiprocessor type, configured for operating with the process according to claim 1 (column 4, lines

Page 10

62-65).

Claim 12

The limitations of process claim 12 correspond to the limitations of claims 1, 3

and 6 and are rejected in the same manner.

Claim 13

Menezes disclosed the process of claim 12, wherein the execution of programs

comprises directing of the instruction sets to said processors of said plurality

according to the priority bits encoded into the said instruction set (column 1,

lines 14-17, multiple execution units; column 4, lines 16-27; column 4, line 60 to

column 5, line 6; column 5, line 59 to column 6, line 15; bundles directed based

upon special neutral instruction providing order or "priority").

Claim 14

Menezes disclosed the process of claim 12, wherein said priority is determined

based on the amount of memory required by each of the processors of said

plurality to execute said instruction set (column 6, lines 33-45).

Claim 15

Application/Control Number: 10/612,825 Page 11

Art Unit: 2193

Menezes disclosed the process of claim 12, wherein said priority is determined based on the amount of percentage of maximum power required by each of the processors of said plurality to execute said instruction set *(column 6, lines 33-45)*.

Claims 16-18

The limitations of claims 16-18 correspond to the limitations of claims 12-15 and as such are rejected in the same manner.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (571)-272-3736. The examiner can normally be reached 10:00am - 4:00pm Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571)-272-3756. The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained form either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR systems, see http://pair-direct.uspto.gov. For questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Patent Examiner AU 2193

November 22, 2006